

CHIPDESIGN COLLEGE™

The *Final* step to
SUCCESS



Lecture
FPGA/ASIC Technology
and Design flow

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Lecture Plan

Program Information:

- Program organization
- Recommended literature

Introduction to ASIC/FPGA Design

- Basic chip structure
- Worldwide High-Tech Industry
- Chip design industry and main applications
- VLSI Circuits technologies
- FPGA/ASIC Design/Verification Flow

Course Organization

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Course Material

➤ *FPGA Course Slide Set*

1. Introduction to Chip Design:
 1. VLSI Circuits Technologies and Chip Design Flow
 2. SoC Architecture
 3. VerilogHDL + full FPGA design flow: Your “first” FPGA Project.

➤ *ASIC Course Slide Set*

1. Reference ASIC Project Overview – Specification and Code.
2. Synthesis, Static Timing Analysis (STA), Gate Level Simulation, Reference Project Implementation Stage Environment Overview.

➤ *Reference FPGA and ASIC Projects Design Environment - Soft Copy.*

Time, Location etc

1. Lecture's days and time:

- Every Friday
- From 9.00 to 13.30 (be at time)

2. Course duration - ~5-6 months [bruto], about 120 ac. hours.

3. Address: Ramat Gan, 7 Aba Hilel str., floor 15

1. **Parking for free options:** Yazira and Ahaliav str. (100-200m from CDC)

Program's Grades Structure

➤ *Final grade structure:*

➤ **Project – 40% from the semester grade**

➤ *Each project includes the Design Specs and the Design Environment*

➤ **Exam – 60% from the semester grade**

➤ *Each exam is in American Style (multiple choice) and closed books*

➤ *The minimum required exam's and project's grade is:* **65.**

➤ *The required course average is:* **70.**

Study and Help with Job Search Plan

- *The Course milestones are the Project milestones:*
 - MRD, Kickoff, PDR, CDR, FDR and final exam
- *CV Design - Very effective and professional help*
- *Coaching for successful career building*
 - Time and project management
 - Career planning and Job search plan design.
- *Project FDR with Senior Designers from HT companies*
- *Diploma, Recommendations and Individual meetings for successful job search etc:*
 - CV/Linkedin Profile Design
 - Job search plan design
 - Technical Interview Simulation

Course rules

- Work with **slides** – questions, comments
 - Study environment at home
 - Weekly **Back up**
 - Course **Forum**
 - Documents and code style
 - **Design reviews** and final submission.
 - **Homework** assignments, which will be done individually or in groups.
- ** The main target of the course** is making the students mature enough in Embedded Linux for the industry. Help yourself using internet forums and online documentation.
- ** Students get certificate** if stand successfully in course requirements.

Recommended Literature

1. *Introduction to ASIC Design –*

- Application-Specific Integrated Circuits, Michael John Sebastian Smith (ASBN 0-201-50022-1)
- www.ee.ic.ac.uk/pcheung/teaching/ee3_DSD/

2. *Introduction to Digital Systems*

- Digital Design, Morris Mano (ASBN - 0130621218)
- www.onesmartclick.com/engineering/digital-logic-design.html

3. *Introduction to Computer Systems*

- Digital Logic and Computer Design, Moris Mano (0132145103)

4. *Introduction to Digital Circuits*

- Teach Yourself Electricity and Electronics, Stan Gibilisco

5. *RTL Design with Verilog HDL and Verification Theory*

- Verilog HDL: A Guide to Digital Design and Synthesis, Second Edition, By Samir Palnitkar, (ISBN: 0-13-044911-3)
- Verilog Language Reference Manual (Open Verilog International)
- VCS User Guide
- ModelSim User Guide

Recommended Literature

6. *Synthesis Theory*

- Logic Synthesis Using Synopsys, Pran Kurup, Taher Abbasi
- Design Compiler User Guide

7. *STA Theory*

- Prime Time User Guide

8. *TCL and Linux Literature*

- Using Tcl With Synopsys Tools
- Linux Red Hat Getting Started Guide: Shell Prompt Basics

Program Plan – FPGA Part

- **VLSI Circuits Technology Overview**
- **Chip Design Detailed Design Flow**
- **RTL Design with VerilogHDL**
- **Verification with VerilogHDL**
- **Simulator tool – Theory and Practice (ModelSim of Mentor Graphics)**
- **SoC (System on Chip) Architecture overview**

Program Plan – FPGA Part2

- **FPGA Implementation Design Stage (Theory and Practice):**
- **Synthesis and P&R tool – Theory and Practice (Quartus, Altera)**
- **Coaching for success in career**
- **“Reference” FPGA Project Review (GPT)**
- **“First” FPGA student’s project design – DMA IP as AMBA peripheral device of SoC**

Adv. Course Plan – ASIC Course

- **“Ref” ASIC Project Review**
 - Design and Verification Spec
 - Code Review
- **Introduction to Linux - Theory and Practice**
- **Start “First” ASIC Project by Engineers**
 - Architecture
 - RTL Design and Integration
 - Functional Verification
- **ASIC Implementation Design Stage**
 - Synthesis and Static Timing Analysis (STA).
- **“First” ASIC Project design finishing:**
 - Synthesis/STA
 - Timing Simulation.
- **“First” ASIC Project Design Reviews with guests from the industry:**
 - Kick off meeting. PDR. CDR. FDR
- **Coaching and job search plan and material preparation:**
 - Real High Tech Project planning and management
 - The Successful Career building: Job Search Plan, CV design + interview

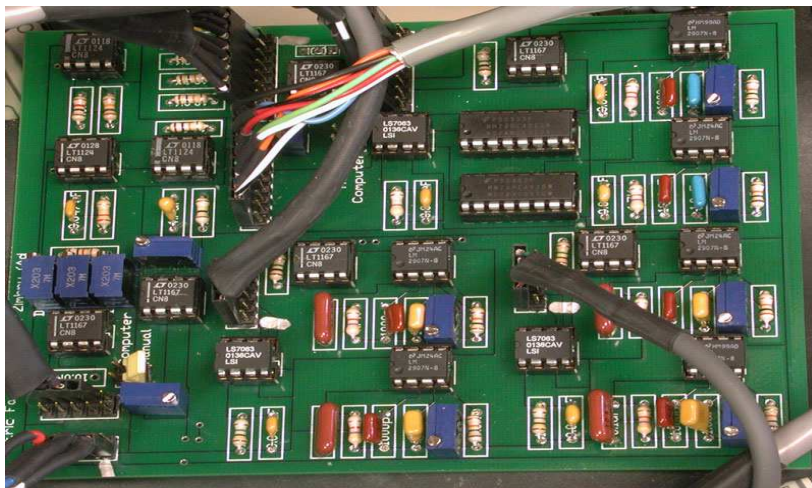
Course Plan – Verification Course

1. Modern Random Test Verification Methodology fundamentals
2. SystemVerilog Test Benches (SVTB) – HVL
3. VCS Simulator Practice
4. SV Advanced subjects (OO, Randomization, Interfaces)
5. SystemVerilog Assertions (SVA)
6. “Reference” Chip Verification Industrial Project Requirements and Verification Spec review.
7. Verification Methodology Manual for SystemVerilog Verification (VMM)
8. “First” Chip Verification Industrial Project Requirements (MRD and Kick Off)
9. “Reference” Chip Verification Project RTL Code and Verification Env. Review
10. “First” Chip Verification Project Implementation
11. “First” Chip Verification Project Design Reviews with guests from the industry:
 - Kick off meeting. PDR. CDR. FDR
12. Coaching and job search plan and material preparation:
 - Real High Tech Project planning and management
 - The Successful Career building: Job Search Plan, CV design + interview

What is a chip?

Advantage Vs PCB Design

- **Why IC development led to high-tech revolution?**
- Integrated in one chip circuits (IC) replaces large amount of discrete components on the board.
- **Almost all traditional discrete elements like:**
 - Processors **Digital Discrete Logic**
 - Memories **Analog blocks***can be integrated in one "piece of silicon" – chip*



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Advantage Vs PCB Design

Main advantages of ICs comparing to discrete components:

- **Area** – Integrated circuits are much smaller – both transistors and wires are shrunk to micrometers. Small size leads to advantages in speed and power consumption, since smaller components have much smaller parasitic resistance, capacitance and inductance.
- **Timing** – Digital logic switching, analog effects and communication between blocks in the chip can occur hundreds of times faster than with the discrete components on a PCB.
- **Power Consumption** – Logic operations within a chip also take much less power and allow operating on very low voltage supply (1.8V-> 0.9V)
- **Reliability** - The probability for failure (MTBF) and impact of external environment are much less in integrated circuits compared to discrete components. The lifetime of the product based on IC is much longer than one based on discrete components

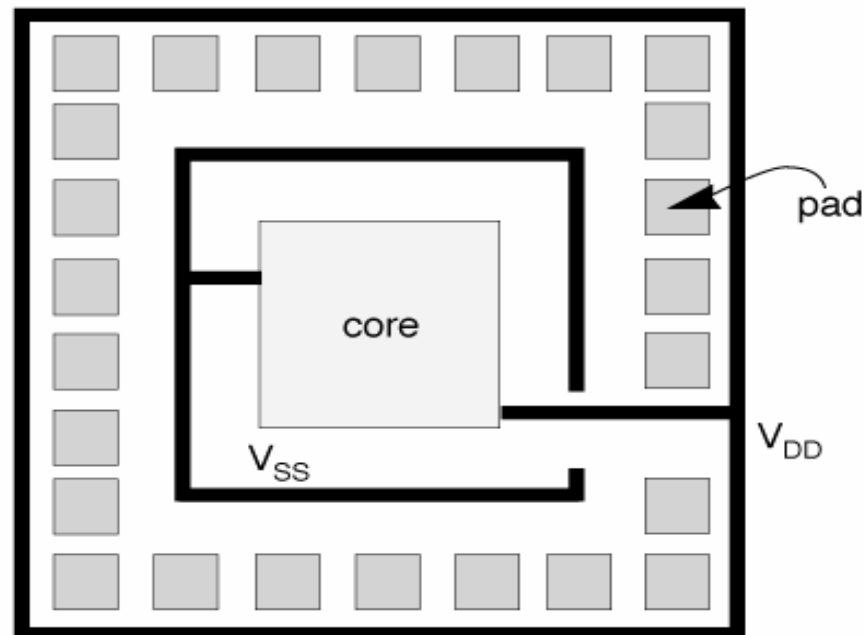
Chip Structure

- *Basic Chip Components:*

Each chip structure contains two regions:

- Core area
- Pads (I/O) area

- *The following picture shows the division of the chip into these regions*



Chip Architecture

Core area design:

- Core area may contain the following main blocks
 - Digital Logic Circuits
 - Analog Blocks (Voltage Regulators, Oscillators, PLLs etc..)
 - On Chip Memory blocks (ROM, SRAM, etc...)

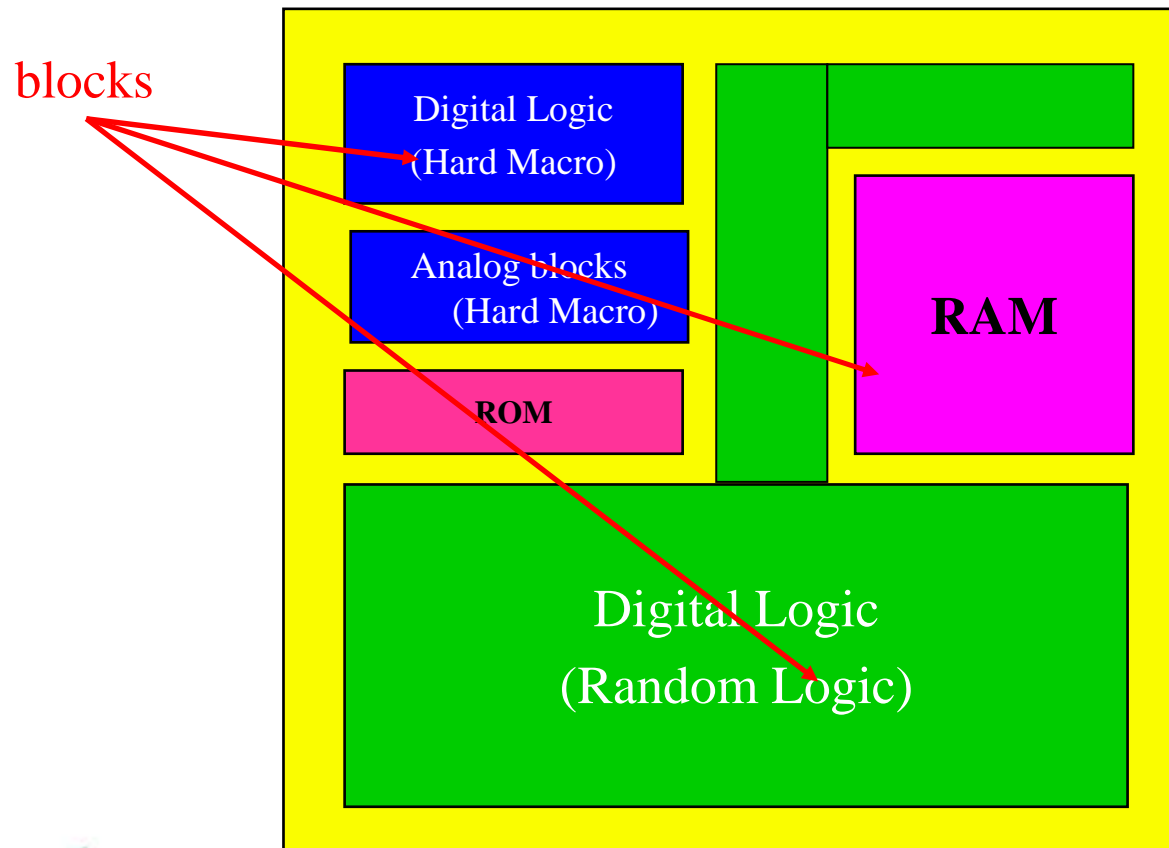
All these blocks are placed in the *core area*. The connection between these blocks is implemented using metal wires.

Voltage supply to these blocks is implemented with *power (VDD and VSS) rings*.

Each chip may have one or more power segments. For example pads and core area may have separate supply rings.

Chip Architecture

The following picture shows the placement of the main blocks inside the core area.



Main Components – Digital Blocks

- *Digital Logic* is implemented on silicon using CMOS transistors and metal (wires) connection between these basic components.
- *Standard technology libraries* are used for implementation of digital logic. These libraries include optimized implementation of basic elements like logic gates (nor, nand, not etc), flip-flops, etc..
- Sometimes when a digital block has a very special requirement it is implemented as a *Hard Macro*. This approach can improve the characteristics of this block, but has negative impact on chip placement.

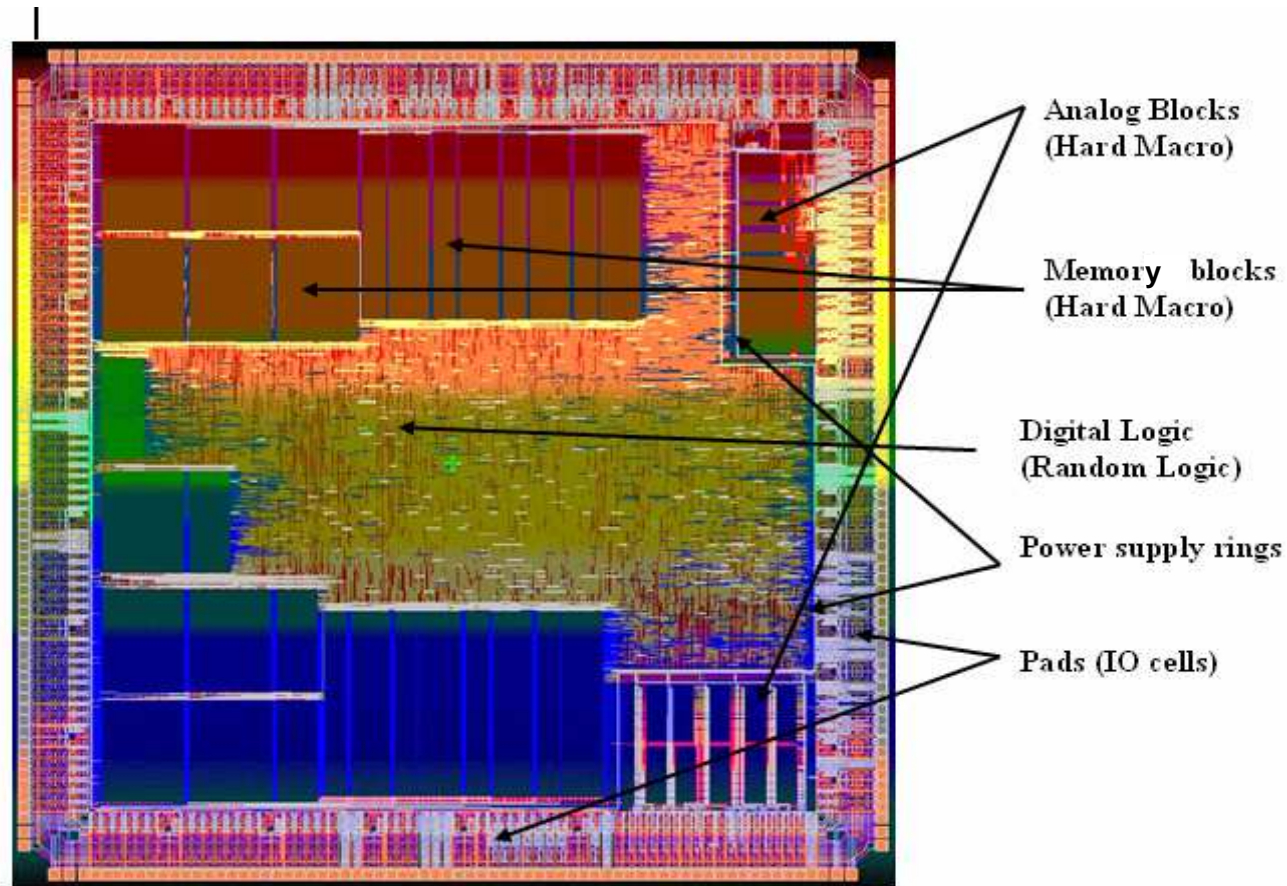
Main Components – Analog Blocks

Analog and mixed signal blocks are always designed in **transistor level**. So, all these blocks are integrated as **hard macros**.

The following blocks are commonly implemented in silicon:

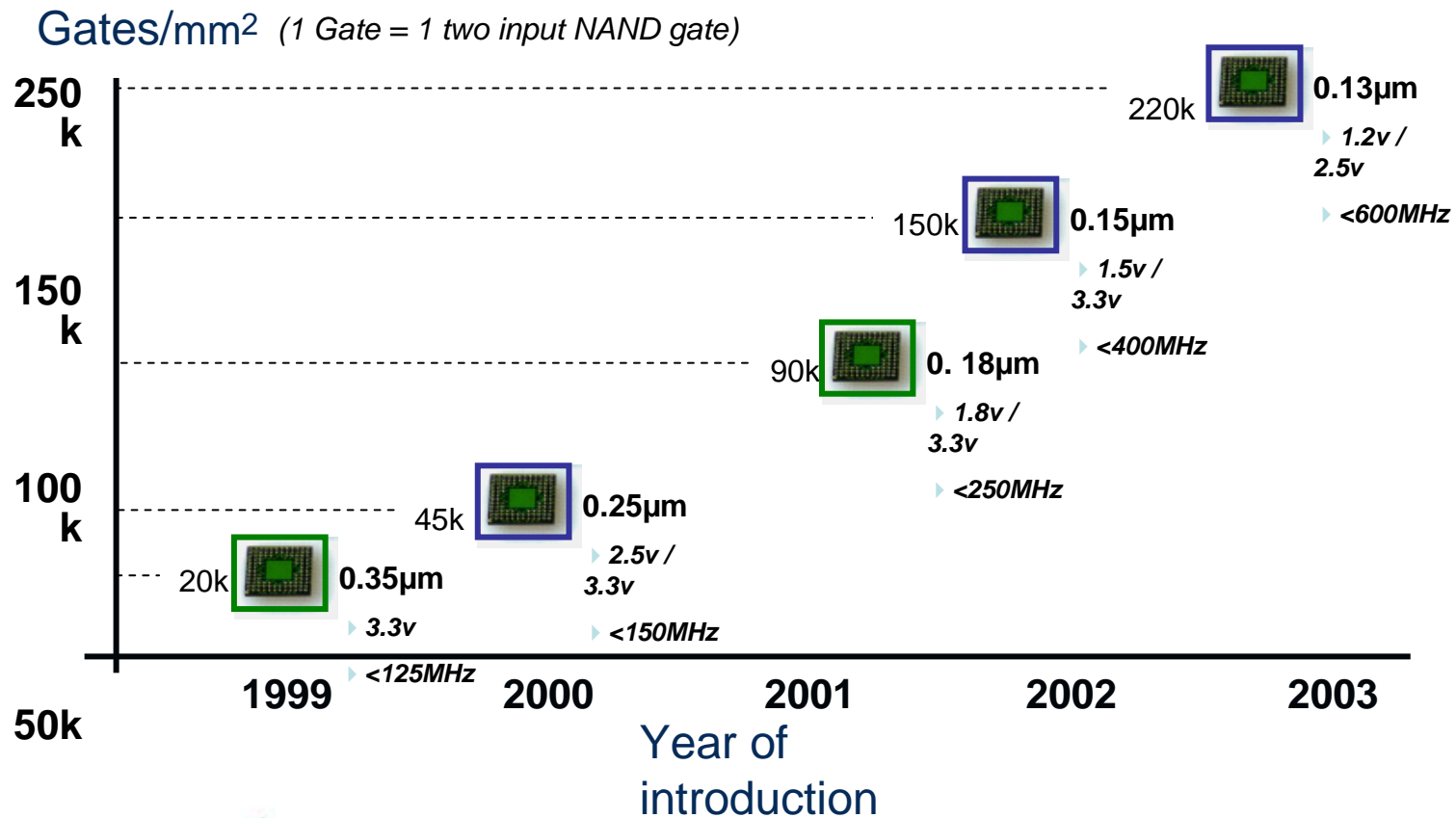
- **Voltage Regulators** – used for voltage supply of internal logic and pads from external power supply. The most popular regulator implemented on silicon in 0.18u process is 3.3V to 1.8V
- **Power On Reset (POR) and Voltage Detectors** – used to generate system reset for on-chip logic during power-up and when external supply is going down and can't provide sufficient voltage level for internal logic.
- **On Chip Oscillators and PLLs:**
Used to create clock for the on-chip logic and systems. Wide range of clock frequencies for the system clock can be generated.
- **Digital to Analog and Analog to Digital Converters:**
Provide interface between the on-chip digital logic and the on-chip or the external analog blocks. Wide range of applications, like audio (MP3) and video, require implementation of these blocks on silicon.

ASIC Example



Introduction to VLSI Circuits Industry

Chip Design History



Chip Design Main Applications

Main players on the market of products based on chips

- Mobile Phones: Nokia, Samsung, Ericsson, Motorola, Philips, LG, Sharp
- Personal Computers: IBM, Dell, Samsung, LG
- PDA's: Palm, HP, Sony etc
- Communication Devices: Cisco, Lucent, etc
- Cameras: Sony, Panasonic, Samsung, Sharp
- Storage devices, MP3 – Sony, Samsung, SanDisk, M-Systems

Main players on the market of Integrated circuits

- Chipsets for mobile phones: Qualcomm, Motorola, Agere, Zoran
- CPUs for Personal Computers: Intel, AMD
- Routers for Communication devices: Nortel, Infineon
- Memories for storage devices: Samsung, AMD, Intel, Toshiba

VLSI Circuits Technologies Contents

- **Technology Overview**
 - VLSI Circuits
 - Full custom, ASIC, FPGA/PLD.
 - Main principles & trade-offs

VLSI – ASIC and PLD

VLSI Circuits - Very Large Scalable Integrated Circuits:

Modern chips, contain integrated circuit with hundreds of thousands or even millions of transistors are called – *VLSI Circuits*

VLSI Circuits are divided to:

- Programmable Logic Devices (PLD)
- Non programmable – Application Specific IC (ASICs)

ASIC – Application Specific Integrated Circuits:

Most of the integrated circuits (not PLD) are designed to support specific, well defined functionality (CPU, control systems, algorithms, standards, protocols etc..).

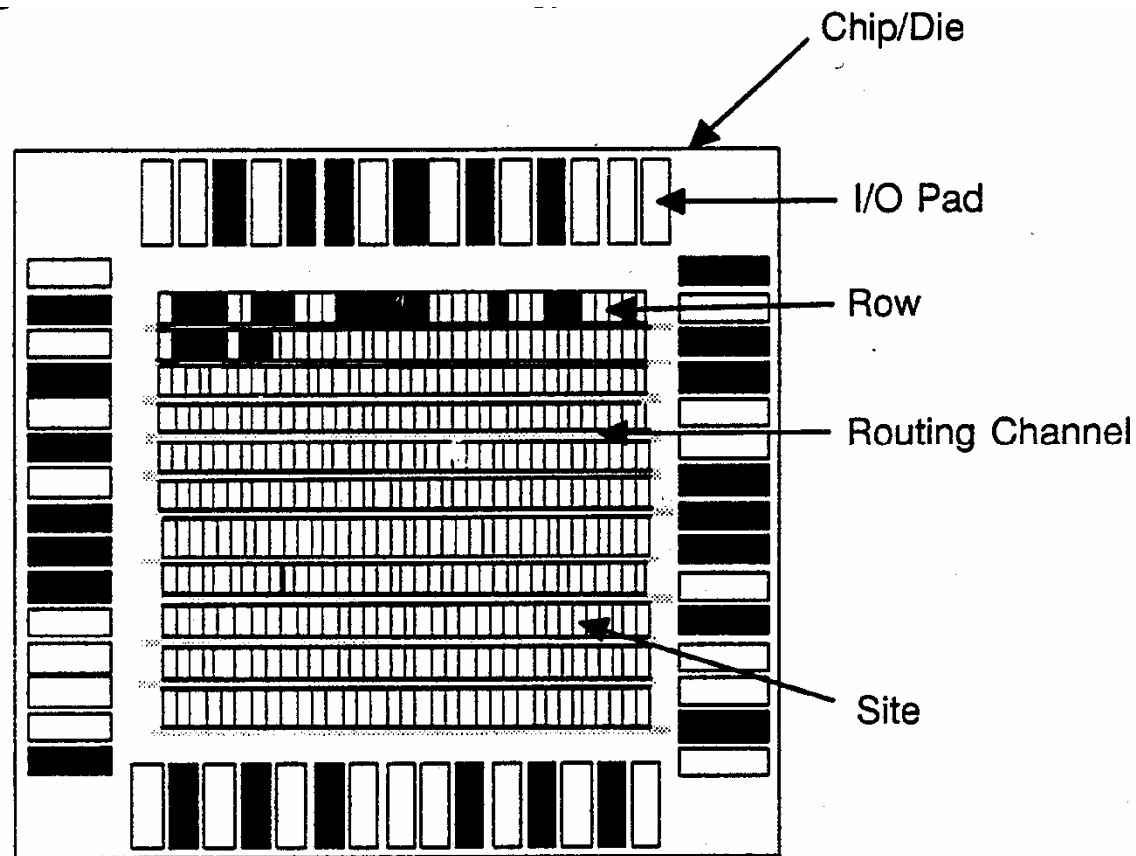
PLD – Programmable Logic Devices:

For prototypes design and for non mass production markets the programmable chips – FPGA/CPLD are used.

CPLD – Complex Programmable Logic Device

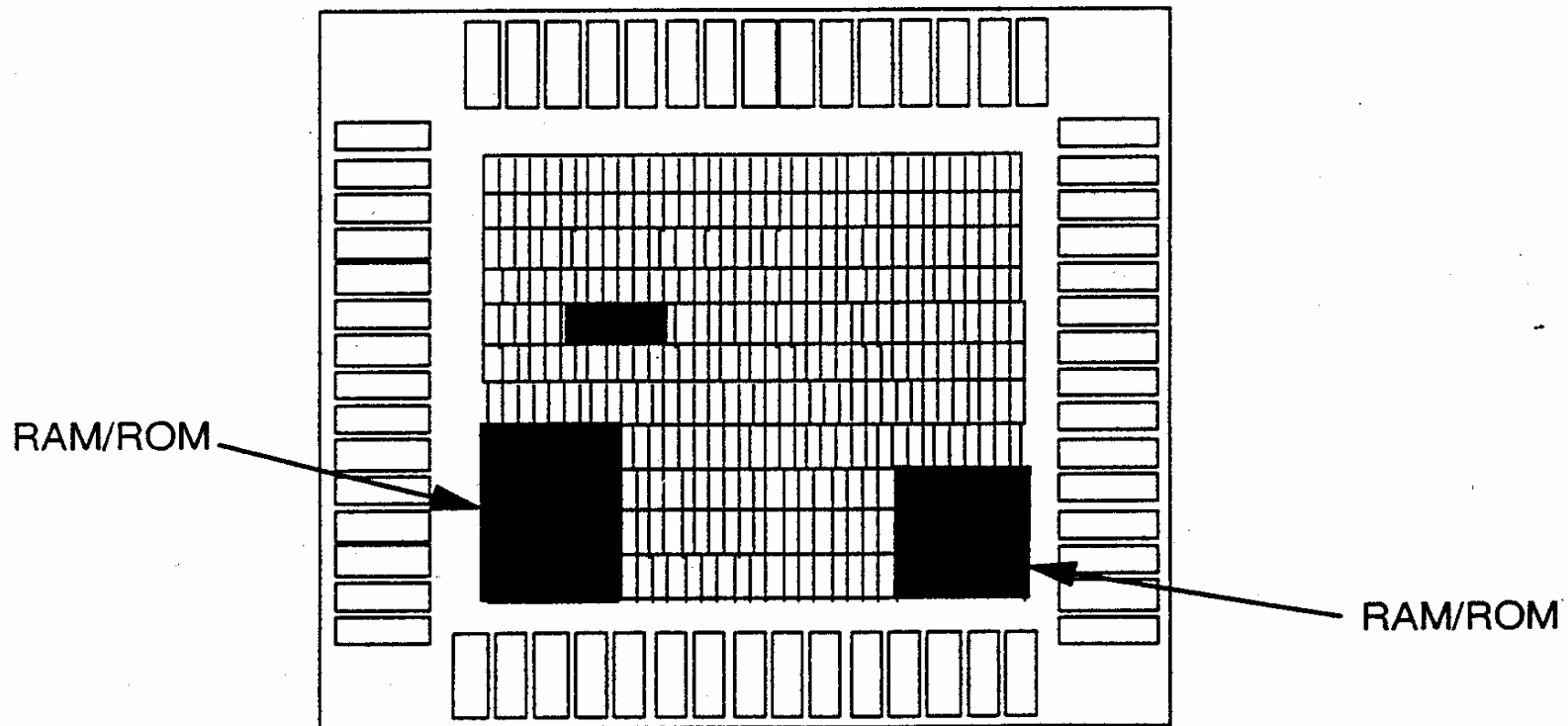
Full Custom Integrated Circuits

A structure of a full custom IC is shown in the following figure:



Semi-Custom Integrated Circuits

A structure of a Semi-Custom IC is shown in the following figure:



Programmable Logic Devices

➤ Programmable Logic Devices

- PLD (FPGA/CPLD) chips have a very general structure and include a collection of programmable switches that allow the internal circuitry in the chip to be configured in many different ways.
- The designer can implement whatever functions are needed for a particular application by choosing an appropriate configuration of the switches. PLDs can be programmed multiple times.

Programmable Logic devices

Advantages:

- *Flexibility - reprogramming*
- *Time To Market – TTM*
- *Low cost solution for small quantities*

Disadvantages:

- *High cost solution in large quantities*
- *Not so high integration -> large area and poor performance*
- *Not flexible in terms of integrating analog blocks*

PLDs are available in a wide range of sizes up to 10 M gates

These chips consist of a large number of small logic elements, which can be connected together using programmable switches

Programmable Logic devices

Two of the most sophisticated types of PLD are known as CPLD (Complex PLD) and FPGA (Field Programmable Gate Arrays).

The main difference between CPLD and FPGA device is the internal architecture:

- CPLD devices are based on E2PROM cells. These cells are not erased when voltage supply is disconnected.
- FPGA devices are based on a Static RAM (SRAM) basic cells, which contain the data only when voltage supply is connected.
- FPGA cells are based on lookup table – truth table of the function
- CPLD cells are based on sum of products (concept of PAL)

Programmable Logic Devices

Structure of a basic FPGA cell (Configurable Logic Block)

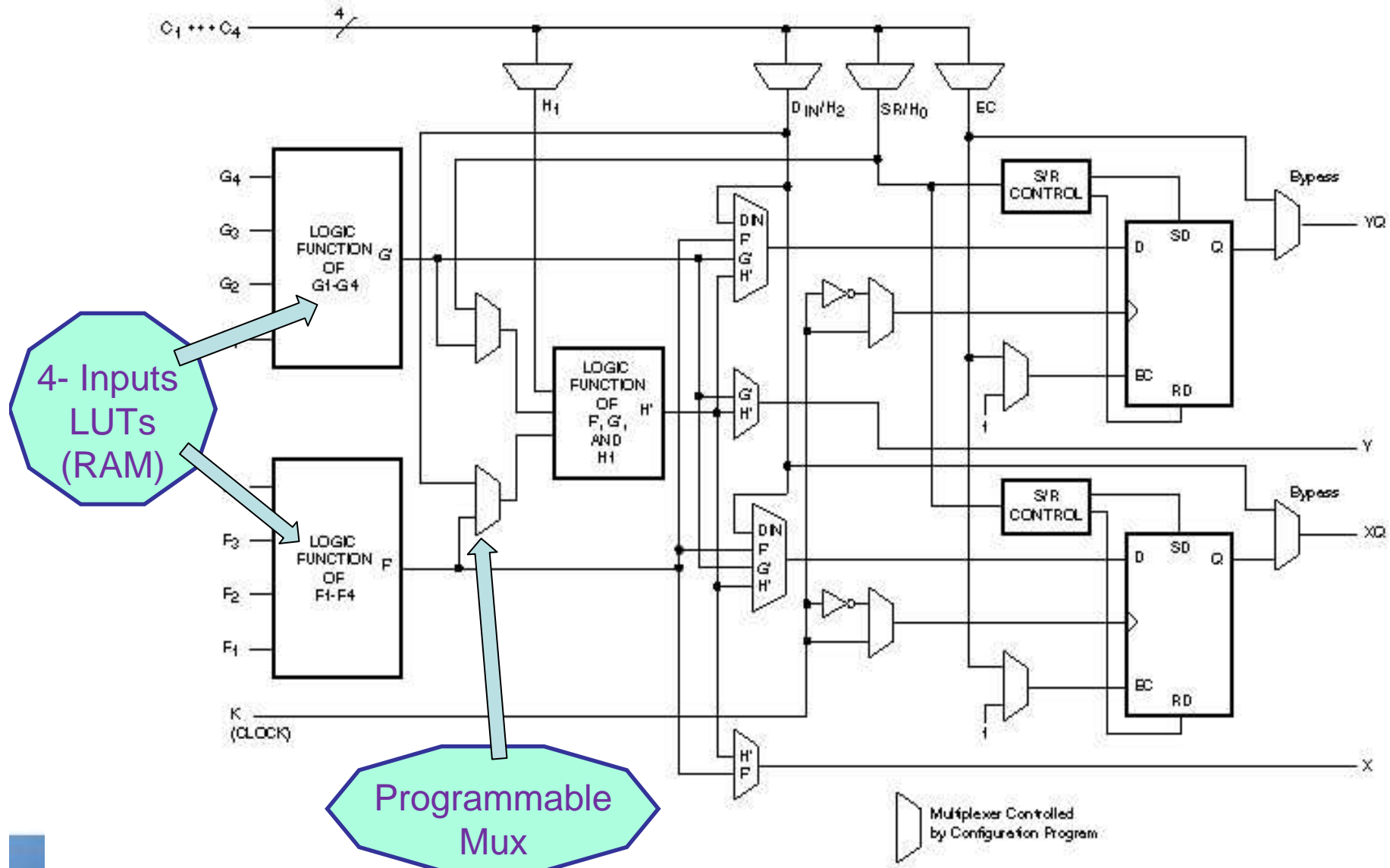


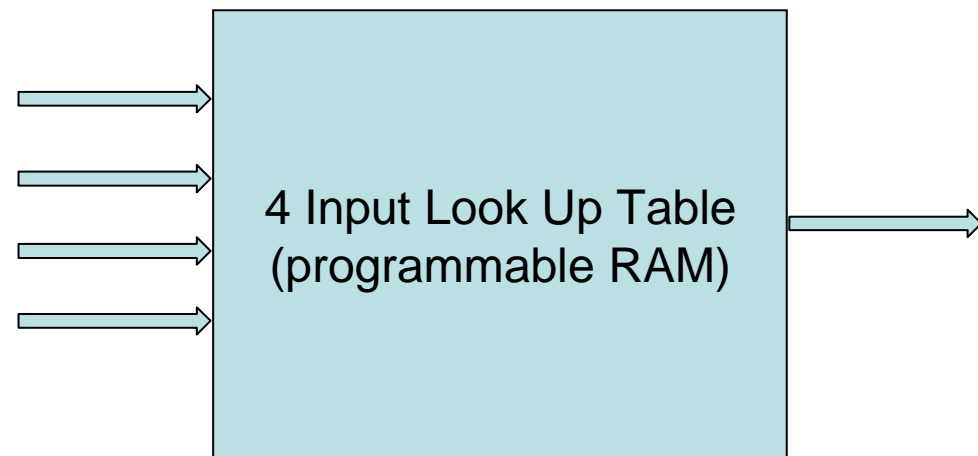
Figure 1: Simplified Block Diagram of XC4000-Series CLB (RAM and Carry Logic functions not shown)

Programmable Logic Devices

4-input look up table (LUT) implements combinational logic function.

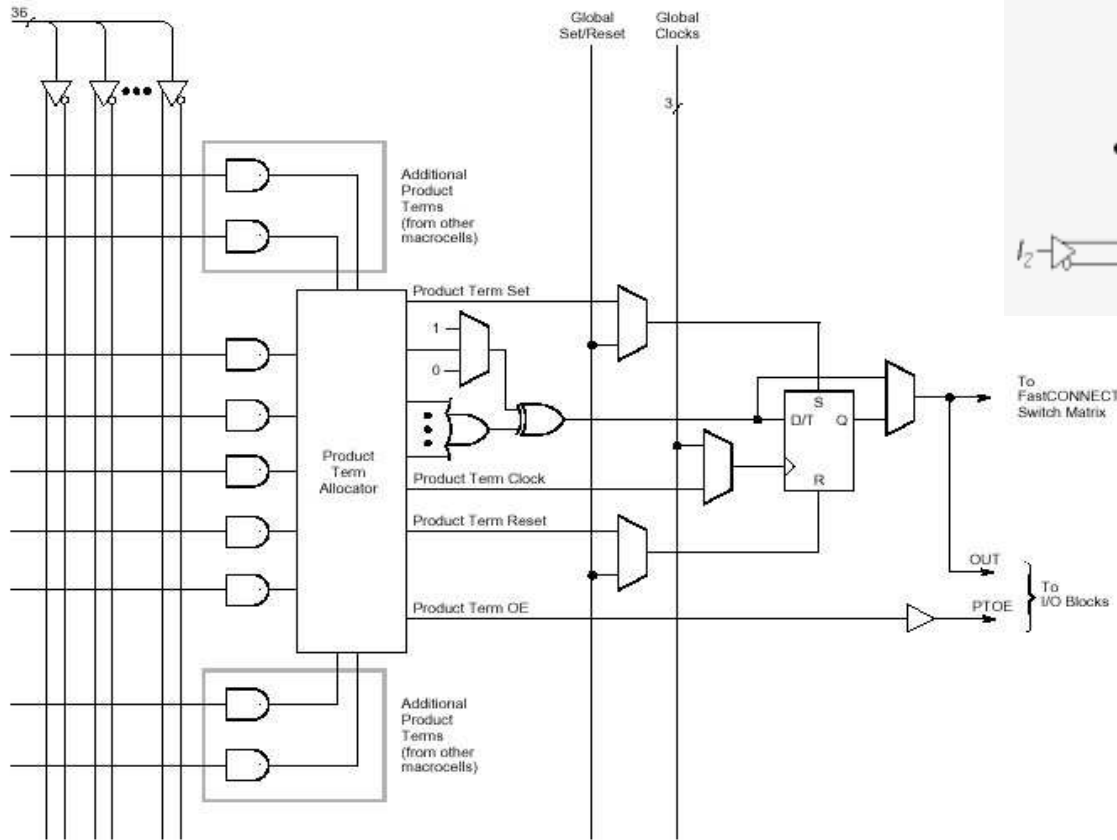
2^4 memory *cells are required to implement $2^{(2^4)}$ different functions*

Inputs	AND	F1	F2
0000	0	1	0	
0001	1	0	0	
0010	1	1	0	
0011	1	1	1	
0100	1	0	1	



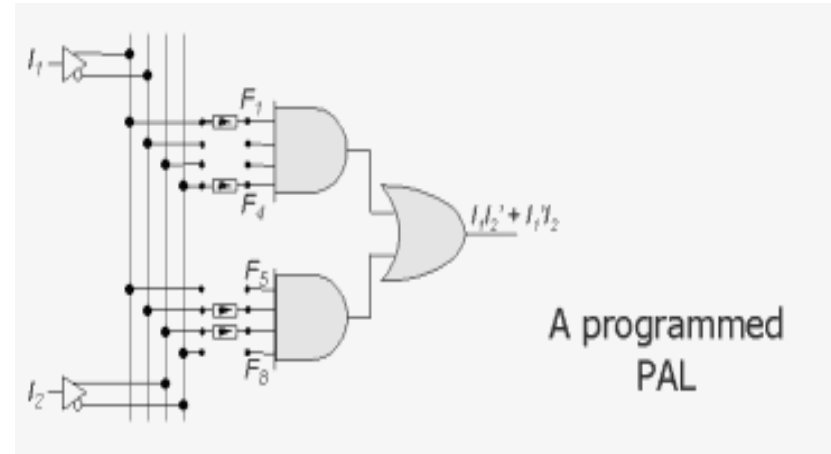
Programmable Logic Devices

Structure of a basic CPLD cell



cr

XC9500 Macrocell Within Function Block



Programmable Logic Devices

- **System On a Programmable Chip:**

Modern FPGA devices include various number of hard macros- full custom design, such as

- **Memories** (Different kinds of RAMs, FIFOs etc..).
- **The size and configuration** of memory blocks can be configured.
- **Total maximum size** of memories can reach several Mbits.
- **Configurable PLLs**, used for clock multiplexing.
- **Popular CPUs**, like ARM, optimally implemented as hard-macro.

Programmable Logic Devices

Main semiconductor companies producing PLD:

- *Xilinx*
- *Altera*
- *Lattice, Actel, Atmel*

In some cases PLDs are not able to meet the desired performance, power consumption or cost objectives.

In such situations it is possible to design a chip from scratch in the following way:

- ✓ *The logic circuitry design*
- ✓ *Appropriate technology choice – synthesis with special technology libraries*
- ✓ *Chip is manufactured by a company that has fabrication facilities (FAB)*

ASIC/ FPGA Design Flow Contents

- **Chip Design flow**
 - Chip design stages description.
 - Inputs and outputs of each stage.
 - Chip production.

Detailed Chip Design Flow

Main stages of the ASIC Design project:

- Marketing Requirements Specification (MRS)
- Project Initialization Stage
- Specification stage
- Logic Design Stage
- FPGA Implementation and Validation Stage (optional)
- ASIC Implementation Stage
- Tape-Out - Transfer to FAB (Transfer to Production)

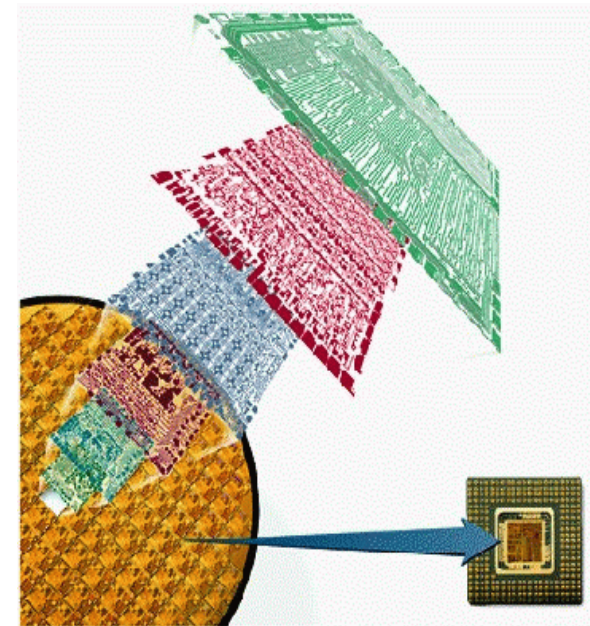
Chip Manufacturing

Fabrication:

Input to fabrication process is Database in GDSII format

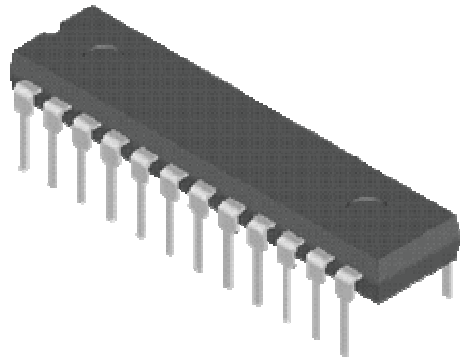
The following procedure is implemented during the manufacturing

- Masks generation
- Silicon wafer preparation, oxidation
- Photolithography
- (expose wafer with UV light via the mask)
- Poly-silicon layers creation
- Metallization.
- Wafer post-processing
- Wafer test, sort and cut
- Packaging
- Final test + Silicon testing.
- Qualification



Chip Packaging

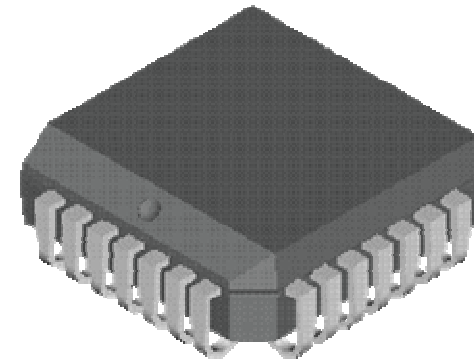
The following pictures demonstrate different types of packages:



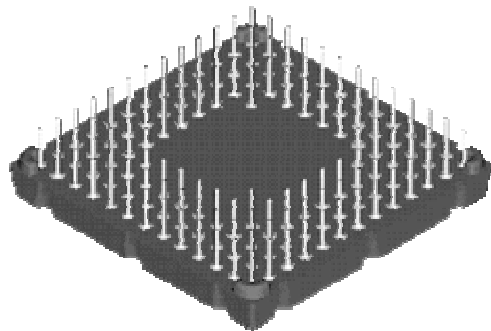
DIP = Dual In Line Package



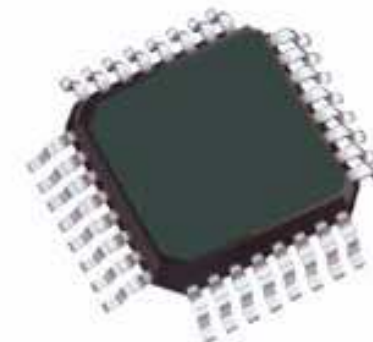
BGA=Ball Grid Array



PLCC=Plastic Leaded Chip Carrier



PPGA=Plastic Pin Grid Array



QFP=Quad Flat Package

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